FET cascode technique optimizes differential amplifier performance

Low-cost FETs afford breakdown voltage protection, while common mode rejection ratio and other circuit parameters can be improved by a factor of 100 without closely matched bipolar transistors or expensive components

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☐ The usual tradeoffs encountered in low-frequency linear circuit design often result in less-than-satisfactory overall performance. But a self-biasing cascode arrangement, in which an amplifier device is isolated from its load by a depletion-mode field effect transistor, offers an improvement factor of up to 100 in many critical performance characteristics without adversely affecting others. And best of all, the circuit can be constructed using an inexpensive, garden-variety FET.

In the cascode arrangement, the FET carries the burden of the breakdown voltage specification, while the amplifier device itself sees only the much lower operating gate-to-source voltage. The amplifier's output admittance and its feedback ratio in this stage are reduced by a factor equal to the mu of the cascoded FET.

The technique is based on the depletion-mode FET in a grounded gate circuit shown in Fig. 1. The n-channel junction FET, Q_1, is a depletion-mode device, so the source will be more positive than the gate if the current through the device is less than I_{DSS} (drain current with the gate shorted to the source). With signal current I_S on, the FET's gate-to-source voltage will stabilize at a potential between zero and pinch-off, usually 1 or 2 volts.

A feature of the grounded-gate FET circuit is its precise unity current gain. With only a few nanoamperes of gate leakage current, I_{GSS}, flowing through the gate electrode, nearly all the current from source I_S flows through Q_1 into the load resistor, R_L. The result: no error currents. The voltage appearing across the current source is equal to the 1 or 2 volts of operating gate-to-source voltage. But the output voltage appears between the drain and gate of Q_1; it's limited only by the drain-to-gate breakdown voltage of Q_1, which can be as high as 300 V.

Now it's evident that at the cost of introducing an error that is typically less than 1 part per million, the breakdown voltage applied to the current source, I_S, has been reduced to a few volts, while the voltage breakdown capability of the composite current source of I_S and Q_1 has been increased to the breakdown limit of Q_1.

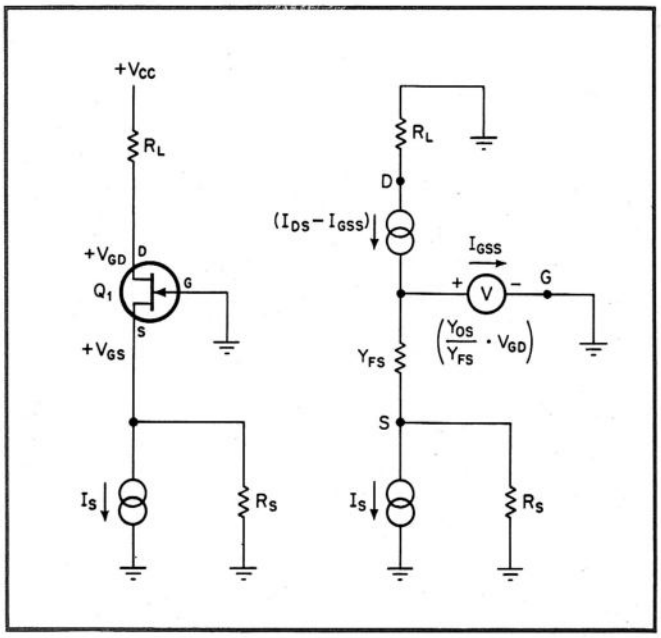
Another advantage is a reduction in the voltage change seen by I_S for a given change in output voltage. This reduction is expressed as

$$\frac{\Delta V_{GS}}{\Delta V_{GD}} = \frac{Y_{OS}}{Y_{FS} + \dfrac{1}{R_S}} \leqq \frac{Y_{OS}}{Y_{FS}} = \frac{1}{\mu}$$

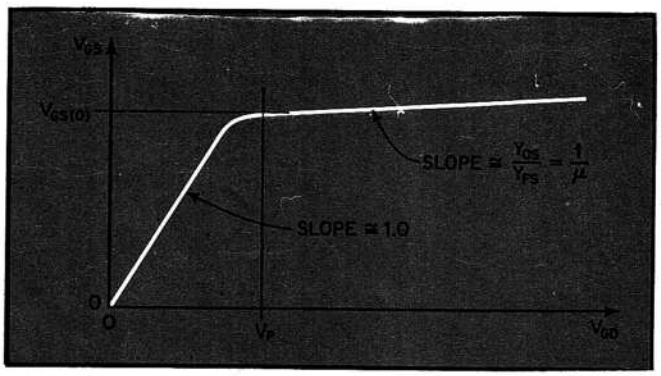
provided that $V_{DG} \geqq V_P$, where V_{GS} is gate-to-source voltage; V_{GD} is drain-to-gate voltage; Y_{FS} is forward transconductance; Y_{OS} is output admittance; R_S is signal current source output impedance $\mu = Y_{FS}/Y_{OS}$, and R_P is pinch-off voltage.

The reduction factor, $\Delta V_{GS}/\Delta V_{GD}$, compares with the ratio of the FET's output admittance to transconductance—typically a factor of 0.01. The result: the small-signal output impedance of the composite current source of I_S and Q_1 is at least 100 times larger

1. Protection. Basis of cascode technique is the grounded-gate FET. Current source I_S is isolated from supply voltage by FET Q_1. Operating gate-to-source voltage of Q_1 usually amounts to only 1 or 2 volts and only voltage change felt by I_S is $(Y_{OS}/Y_{FS})V_{GD}$ or V_{GD}/μ. FET's output voltage is limited by its breakdown characteristics and appears between the gate and drain of Q_1. Leakage current through FET, I_{GSS}, runs to only a few nanoamperes, so almost all the current from I_S flows through Q_1 and R_L.



2. Linear range. Characteristic of a typical FET shows that when drain-to-gate voltage, V_{GD}, falls below pinch-off voltage, V_P, gate-to-source voltage decreases and FET appears as a series resistance. If FET is to act as a linear device and perform desired isolation function, operation must be set at point where slope is $1/\mu = 0.01$.

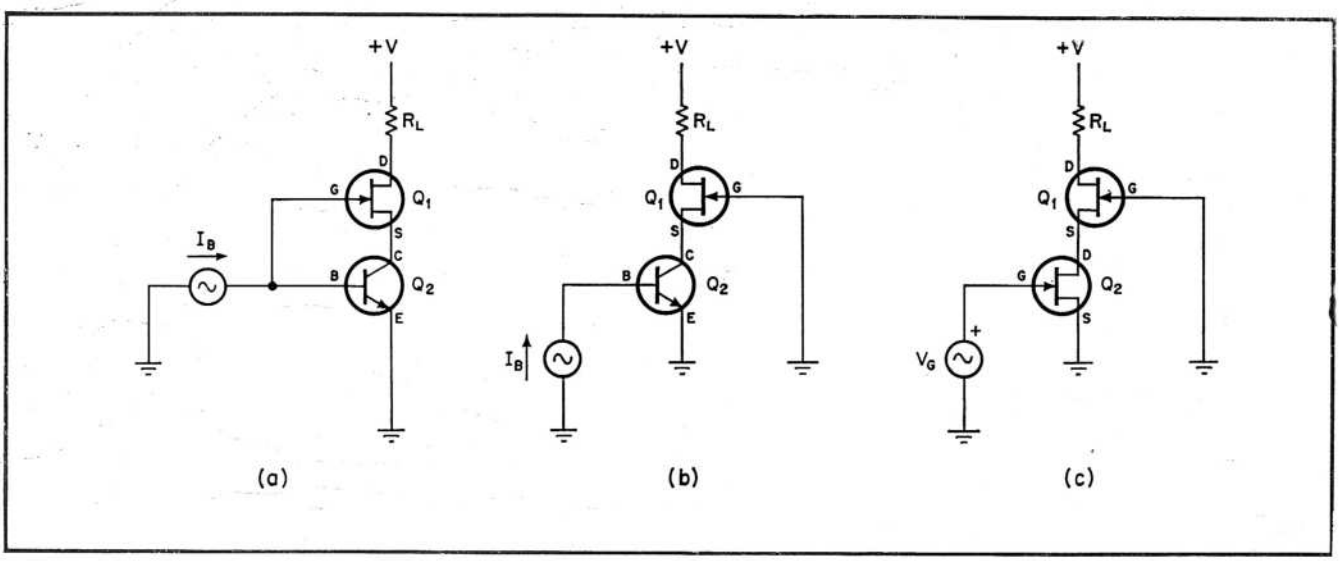


begins to look more like a switch than a linear FET, the improvement ratio will fall toward 1.

The FET cascode technique may be applied to bipolar transistors and FETs, as shown in Fig. 3 The quasi-cascode approach (Fig. 3a) applied to a bipolar transistor with the FET in the gate-base mode works for any combination of bipolar transistor and FET. However, the FET's rated I_{DSS} must exceed the maximum current passing through Q_2.

This method also can be used to improve the bipolar transistor's ac characteristics. Here the FET's gate-to-drain capacitance effectively replaces the bipolar's collector-to-base capacitance. The transistor's actual collector-to-base capacitance is reduced by an amount equal to $1/\mu$. This effect can be used in differential amplifiers to improve their high-frequency common-mode rejection ratio (CMRR).

Similarly, with the true cascode circuit (Fig. 3b) the bipolar transistor's ac characteristics are further



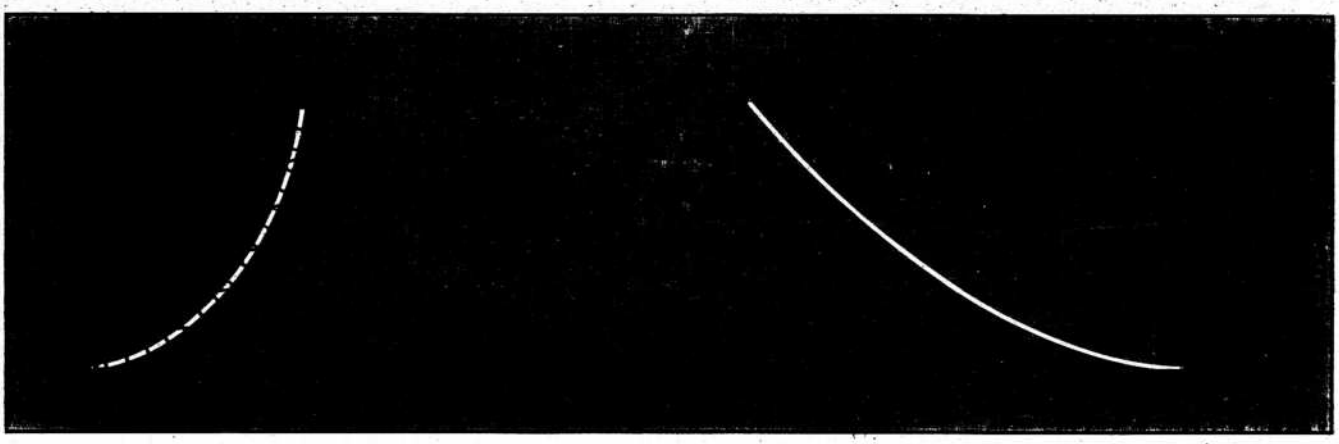
3. Three variations. Quasi-cascode circuit (a) has features of true cascode—bipolar transistor's output is isolated from load by FET. Dc characteristics of bipolar transistor are improved if I_{DSS} of Q_1 exceeds maximum current through it. Bipolar/FET configuration (b) is true cascode—it has grounded-emitter input and grounded-gate output. Collector-to-base capacitance of Q_2 is reduced by improvement factor, $1/\mu$, of Q_1, thereby improving bipolar's ac performance. FET/FET cascode (c) is similar to bipolar/FET cascode since equivalent terminals are connected in a like manner.

than that of I_S alone. If I_S is a FET or a bipolar transistor, the small-signal characteristics related to output voltage change, such as output admittance and feedback ratio, are effectively reduced by a factor of 100.

However, as indicated in the equations, a practical limitation does exist. The dc drain-to-gate voltage of Q_1 must at least equal the pinch-off voltage of Q_1 to achieve the small-signal parameter improvements shown in Fig. 2. If the output voltage falls below this value, Q_1 will enter the resistive region; and, as Q_1 improved, while the same dc improvements are provided in the gate-base model. Likewise, the effective collector-to-base capacitance of the bipolar/FET circuit is reduced as before. There's one consideration, however: Q_1 must be selected for a gate-to-source voltage larger than the emitter-to-base voltage of the bipolar transistor, Q_2, so that Q_2 does not saturate.

The quasi-cascode configuration provides a dc biasing advantage over its true cascode counterpart: in the quasi-cascode setup, any FET will work provided its I_{DSS} is equal to or greater than the current through the bipolar transistor (without considering the gate-to-drain voltage of the FET). In the true cascode circuit, the FET's gate-to-source voltage must be greater than the transistor's base-to-emitter voltage; otherwise the transistor will saturate.

On the other hand, the true cascode circuit offers an ac signal advantage over the quasi-cascode configuration, where a voltage swing across R_L can be coupled through the FET's gate-to-drain capacitance, causing current to flow in the transistor's base. High-frequency gain is reduced because the direction of



4. Finding a FET. Cascode FET for a FET/FET circuit is selected from transfer characteristic curves. Amplifier FET's operating current is chosen first; pinch-off voltage, V_P, then is determined from I_{DS}-V_{DS} curves. Since cascode FET's operating current equals amplifier's, V_{GS} of cascode FET is determined from its I_{DS}-V_{GS} curve; it should exceed pinch-off determined from I_{DS}-V_{DS} curves.

current flow is opposite to that of circuit current. In the true cascode circuit, high-frequency current between the FET's drain and gate flows directly to ground rather than to the transistor's base. What's more, adding the FET reduces the limiting effect of the collector-to-base capacitance of the transistor, resulting in improved high-frequency performance.

The FET/FET cascode circuit (Fig. 3c) is equivalent to the bipolar/FET cascode model. The gate of FET Q_1 is connected to the source of FET Q_2. Q_1's gate-to-source operating voltage should be equal to or greater than the operating pinch-off voltage of Q_2 to assure that Q_2 will remain in the pinch-off region.

In the FET/FET cascode setup, Q_1 can be selected for a given Q_2 by using the voltage-current curves of Fig. 4 (shown here for a typical depletion-mode junction FET). First Q_2's operating current is chosen according to overall circuit requirements, then pinch-off voltage is determined from the I_{DS}-V_{DS} curve. Since Q_1's and Q_2's operating currents are equal, Q_1's operating gate-to-source voltage is determined from the I_{DS}-V_{GS} curves using the value of I_{DS}. The resulting Q_1 gate-to-source voltage should exceed the previously determined Q_2 pinch-off voltage. (It usually will, if the specified maximum V_P or I_{DSS} for Q_1 exceeds those of Q_2.)

Applications, of course, are where circuit designs bear fruit. The differential amplifier circuit shown in Fig. 5 offers a good example. If the mu's of cascode FETs Q_{1A} and Q_{1B} are 200, and they are approximately as well matched as the mu's of the differential amplifier pair, Q_{2A} and Q_{2B}, the circuit CMRR will show an improvement of 40 dB. Even with a minimum amplification factor, (mu of 100 for Q_{1A} and 300 for Q_{1B}) and an initial match of Q_{2A} and Q_{2B} to within 5%, the improvement will be 14 dB.

In a second application shown in Fig. 5, FET Q_3 has been added to the matched-pair bipolar transistor current source Q_{4A} and Q_{4B}. The current source's output impedance is increased by as much as 100. What's more, another source of common-mode error—effect of common-mode voltage on differential amplifier operating current—is greatly reduced by this method.

If FETs Q_{1A}, Q_{1B}, and Q_3 are selected for high voltage (300 V), the differential amplifier can have a common-mode voltage range of ± 100 V with a CMRR typically 10 to 20 dB better than that from the Q_2 pair alone in a conventional low-voltage circuit.

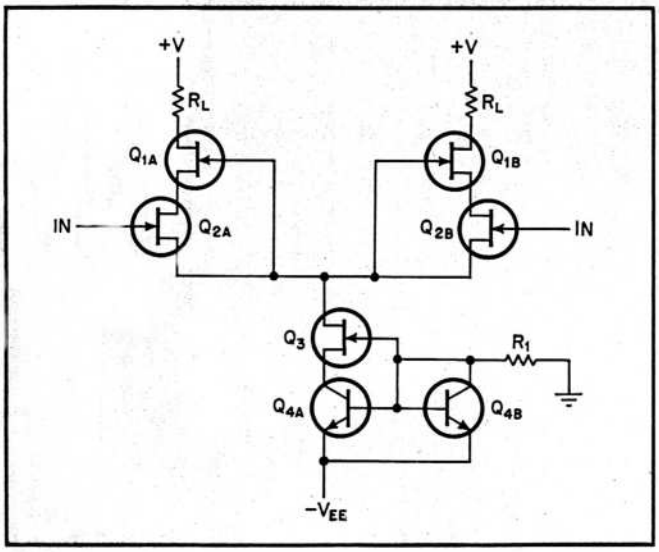
In Fig. 6 a second cascode stage—Q_{5A}, Q_{5B}, and Q_6—is added to the FET/FET cascode differential amplifier shown in Fig. 5. The result: an additional 40 dB of CMRR. However, if FETs Q_{1A} and Q_{1B} have been mismatched, some degradation occurs. Thus, the net improvement is 14 dB from the unbalanced Q_1 and 40 dB from the added Q_5 for a total gain of 54 dB in CMRR over the plain differential amplifier.

In this application transistor Q_5 must be so chosen that its operating gate-to-source voltage exceeds the pinch-off voltage of Q_1, as in the single FET cascode circuit (Fig. 5). In a typical high-voltage differential amplifier, Q_{5A} and Q_{5B} are high-breakdown-voltage FETs, usually with high pinch-off voltages. Thus, Q_{1A} and Q_{1B} are chosen as intermediates between FETs Q_5 and Q_2. Bipolar transistors can be substituted for the differential pair, Q_{2A} and Q_{2B}, with similar results. Enhancement-mode metal oxide semiconductor FETs also can be used in place of Q_{2A} and Q_{2B}.

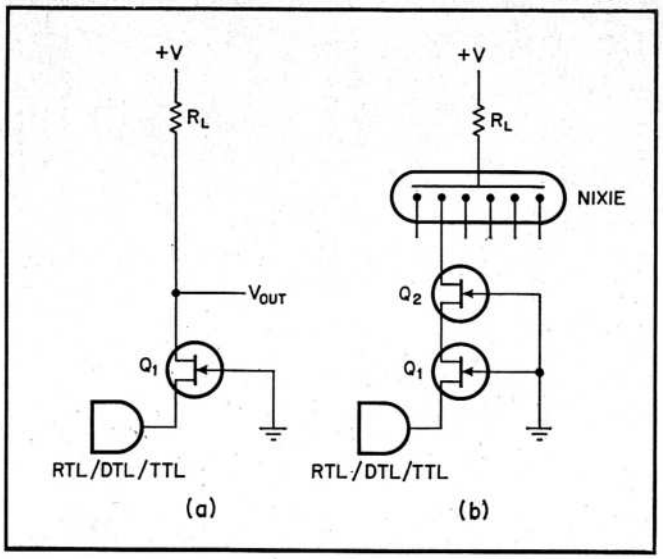
With this approach, the problem of closely matching transistors can be circumvented. But the improvement has its limitations. For instance, a typical bipolar pair has a CMRR of 80 dB. Add a pair of cascoded FETs and the CMRR climbs to 120 dB; with another pair of FETs it's 160 dB. But at this point, other considerations, such as stray capacitance, become limitations, so cascoded FETs cannot be added on indefinitely.

The level converter shown in Fig. 7a is a digital application of the FET cascode approach. Here, FET Q_1 is driven by the output of a logic gate and, in turn, drives a load referenced to a high-voltage supply. This arrangement can be used to interface straight logic with various power supply voltages simply and directly.

Another advantage in this application is that current flow through Q_1 is automatically limited to a value

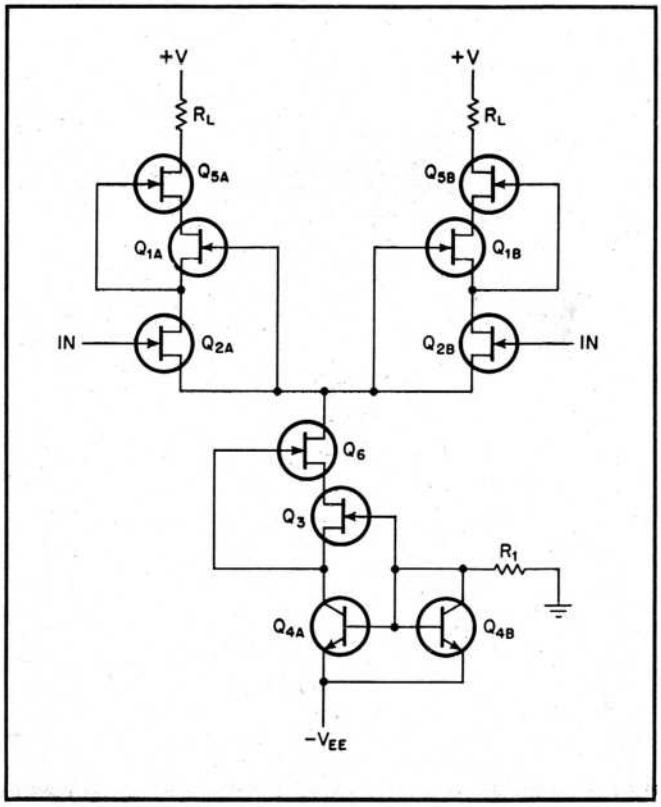


5. Cascode applied. Differential amplifier pair, Q_2, and cascode FETs, Q_1, form FET/FET cascode differential amplifier. Circuit shows significant improvement in CMRR over conventional amplifier. Adding FET Q_3 to matched pair current source Q_4 increases output impedance of Q_4 by a factor of 100. Even if Q_{1A} and Q_{1B} are unbalanced, CMRR still improves by an additional 10 to 20 dB.



7. Digital cascode. FET cascode circuit (a) is level converter that interfaces logic circuits with power supply voltages. Cascode arrangement eliminates high-current spikes and controls peak currents. A variation of this circuit can drive a Nixie tube (b). When logic gate is on, both Q_1 and Q_2 are on, and total resistance is sum of resistances of both FETs. FET Q_2 is a high-voltage type; Q_1 protects logic from high pinch-off voltage of Q_2.

6. Improvements. A second cascode stage, Q_5 and Q_6, improves CMRR another 40 dB. In this multiple FET/FET cascode circuit, Q_5 must be chosen so its V_{GS} exceeds the pinch-off of Q_1; the same is true for Q_6 and Q_3. Bipolar transistors or enhancement-mode MOSFETs can be substituted for Q_2 without affecting circuit performance.



equal to I_{DSS}, useful in interface circuitry to eliminate high-current spikes and to control peak currents. The requirements on Q_1 are sufficient breakdown voltage, I_{DSS} larger than the expected load current, and V_p less than the off voltage of the driving gate.

The technique can also be used to drive a cold-cathode display tube such as the Nixie tube shown in Fig. 7b. Here the circuit calls for a second FET, Q_2, with a high pinch-off voltage. The circuit, in effect, is fail-safe—there is no secondary breakdown, but current limiting is available, an advantage over ordinary Nixie tube drivers. FET Q_1 interfaces between the gate and the high pinch-off voltage of Q_2. When the gate is on, both Q_1 and Q_2 are on; total resistance equals the sum of the on resistance of the two devices. Maximum current is determined by the device with the smallest I_{DSS}.

The cascode technique needn't be costly, even when performance requirements are demanding. For example, in a differential amplifier where the design specifications called for a CMRR of 120 dB and low drift, cost restrictions precluded use of expensive components and trimmer potentiometers. But the circuit requirements were met handily with a pair of 2N4340 FETs in cascode with a standard bipolar dual rated at 80 dB CMRR.

Equally successful was the application to a high-voltage design. With 2N4882s used as cascode FETs, the circuit's CMRR jumped from 94 to 136 dB over a frequency range of dc to 100 hertz. Common-mode voltage range—the maximum voltage that can be applied to the circuit to faithfully reproduce a signal—was improved from ± 20 V to ± 125 V, permitting amplification of small changes in a large voltage. □

February 1, 1966

FET CASCODE CIRCUITS REDUCE FEEDBACK CAPACITANCE

FET cascode circuits bring to solid-state amplifiers the high-frequency characteristics of the pentode vacuum tube. Although FET d-c characteristics are similar to those of the pentode, the FET exhibits an undesirably large Miller feedback capacitance as do all triode devices. Vacuum-tube triodes in cascode have long been used to reduce effective feedback capacitance in unneutralized amplifiers, thus improving stability and bandwidth. FETs operating in cascode accomplish the same results. A FET cascode amplifier, consisting of a common-source and a common-gate stage, is shown in Fig. 1.

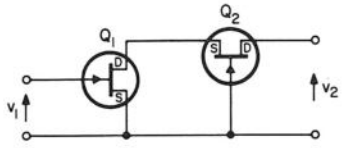


Fig. 1 General Cascode Amplifier

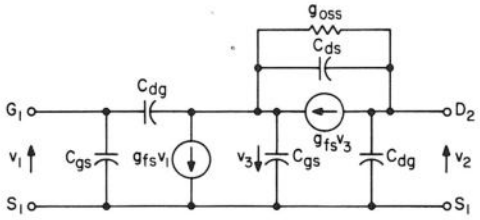


Fig. 2 Cascode Amplifier HF Equivalent Circuit

FET cascode stages provide a hundred-fold reduction in feedback capacitance compared to that of simple FET triode stages. The effective feedback capacitance C_{fb} is then negligible in most applications and circuit performance is limited by layout and shielding considerations as with pentode tubes. The actual value of C_{fb} can be calculated from the complex "y" parameters of the cascode equivalent circuit of Fig. 2. They are:

$$y_{11} = j\omega C_{gs} + \frac{j\omega g_{fs} C_{dg}}{g_{fs} + g_{oss} + j\omega\left(C_{dg} + C_{ds} + C_{gs}\right)}$$

$$y_{12} = \frac{-\, j\omega C_{dg}\left(g_{oss} + j\omega C_{ds}\right)}{g_{fs} + g_{oss} + j\omega\left(C_{dg} + C_{ds} + C_{gs}\right)}$$

$$y_{21} = \frac{g_{fs}^{2} - \frac{C_{dg} g_{oss}}{C_{gs}} + j\omega\left(g_{fs} C_{dg} - \frac{C_{dg}}{C_{gs}} C_{ds}\right)}{g_{fs} + g_{oss} + j\omega\left(C_{dg} + C_{ds} + C_{gs}\right)}$$

$$y_{22} = j\omega C_{dg} + \frac{g_{oss} + j\omega C_{ds}\left(1 + \frac{C_{dg}}{C_{gs}}\right)}{g_{fs} + g_{oss} + j\omega\left(C_{dg} + C_{ds} + C_{gs}\right)}$$

For frequencies below 30 MHz, the denominator functions may be approximated by g_{fs}. Since C_{ds} is approximately zero, the expressions simplify to:

$$y_{11} = j\omega\left(C_{dg} + C_{gs}\right)$$

$$y_{12} = -j\omega C_{dg} g_{oss} / g_{fs}$$

$$y_{21} = g_{fs} + j\omega C_{dg}$$

$$y_{22} = g_{oss} / g_{fs} + j\omega C_{dg}$$

Feedback capacitance is found from y_{12} as $C_{fb} \approx C_{dg} \frac{g_{oss}}{g_{fs}}$

Practical advantages of the FET cascode connection are demonstrated in the gain-bandwidth calculations for an RC-coupled video amplifier. The gain-bandwidth product,

$$GB = \frac{g_{fs}}{2\pi\left(C_{in} + C_{out}\right)}$$

is a measure of amplifier performance. For a single FET stage

$$C_{in} = C_{gs} + \left(1 + A_v\right) C_{dg}$$

$$C_{out} = C_{dg}.$$

The Miller capacitance $(1 + A_v)\, C_{dg}$ presents an effective shunt capacitance proportional to stage gain which seriously limits amplifier performance at high frequencies. As the input stage gain is approximately unity for the cascode connection, then

$$C_{in} = C_{gs} + 2C_{dg} = C_{iss} + C_{dg}$$

$$C_{out} = C_{dg}$$

Using typical characteristics of the Siliconix 2N3368

$$C_{iss} = 7.5 \text{ pF}$$

$$C_{dg} = 2.5 \text{ pF}$$

$$g_{fs} = 2600 \ \mu\text{mho}$$

cascode stage GB is calculated to be

$$GB = 33 \text{ MHz}$$

With a load resistance of 3.9K, the stage gain is

$$A_v = g_{fs} R_L = 10$$

In contrast, the GB of a single amplifier stage at $A_v = 10$ is 11.9 MHz.

An additional improvement in amplifier bandwidth may be obtained by increasing R_L at high frequencies. One technique, called shunt peaking, uses a small inductance in series with the load resistor. The value of inductance for the maximum flat-gain characteristic may be found from the relation[1]

$$L = \frac{R_L^2 \left(C_{in} + C_{out}\right)}{2}$$

An amplifier constructed to test these results appears in Fig. 3. Bandwidth without peaking was 3 MHz; with 75 μH peaking, bandwidth was 6 MHz as shown in Fig. 4. The GB is 36 MHz, which closely agrees with calculated GB of 33 MHz. Similar cascode FET stages may be cascaded to form high-gain video amplifiers without encountering impedance matching problems.

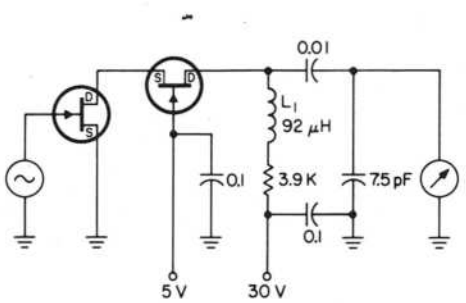


Fig. 3 Wide-Band Cascode Amplifier

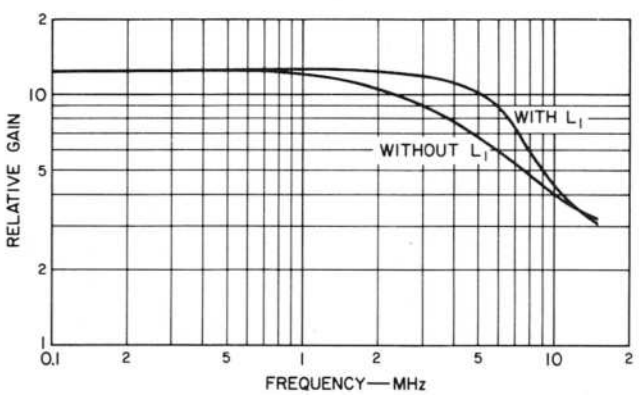


Fig. 4

[1] Terman, F. E., Radio Engineers Handbook, McGraw-Hill, 1943, pgs. 418-420.

Another application of the FET cascode circuit is the 45-MHz amplifier of Fig. 5. If equal Q circuits are desired at the input and output, the required Q is 5 for a 5.7 MHz bandwidth. Using the FET characteristics given above, the input and output circuit constants for a 50 Ω source and load may be calculated:

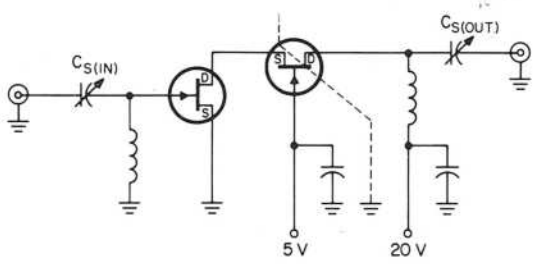


Fig. 5 45-MHz Amplifier

$$C_{s(in)} = \frac{1}{2\omega R_s Q} + \sqrt{\frac{1}{(2\omega R_s Q)^2} + \frac{C_{in}}{\omega R_s Q}} = 10.37 \text{ pF}$$

$$R_{in} = 1/\omega^2 \left(C_{s(in)} + C_{in}\right)^2 R_s = 2.38K$$

and for the output circuit

$$C_{s(out)} = 8.9 \text{ pF}$$

$$R_{out} = 3.2K$$

Using these values the power gain may be calculated as

$$G_P = g_{fs}^2 \, R_{in} R_{out} = 52 \text{ or } 17 \text{ db}$$

since the real part of input and output impedance for the FET is negligible at this frequency.

For any two FETs in d-c cascode, the FET with the higher I_{DSS} value must be used in the output section. This ensures that, for the d-c series connection, neither FET will operate with the gate forward biased at any time.

The most important point in favor of the cascode FET stage is that the feedback capacitance is very low. This improves the frequency response of wide-band amplifiers and eliminates the need for neutralization in tuned amplifiers, thus permitting greater freedom in circuit design.

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